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[TESTING AND REPAIR METHODOLOGY FOR MEMORIES HAVING REDUNDANCY]

Abstract

A method of testing and repairing an integrated circuit having a total number of fuses for effecting repair of the integrated circuit. The method including: testing a memory array with a set of tests and reserving a first number of the total number of fuses for use in repairing the memory array based on results of the first set of tests; and shmoo testing the memory array by incrementing, decrementing or incrementing and decrementing values of a test parameter until a minimum or maximum value of the test parameter is reached that utilizes a second number of the total number of fuses for use in repairing the memory array to operate at the minimum or maximum value of the test parameter.